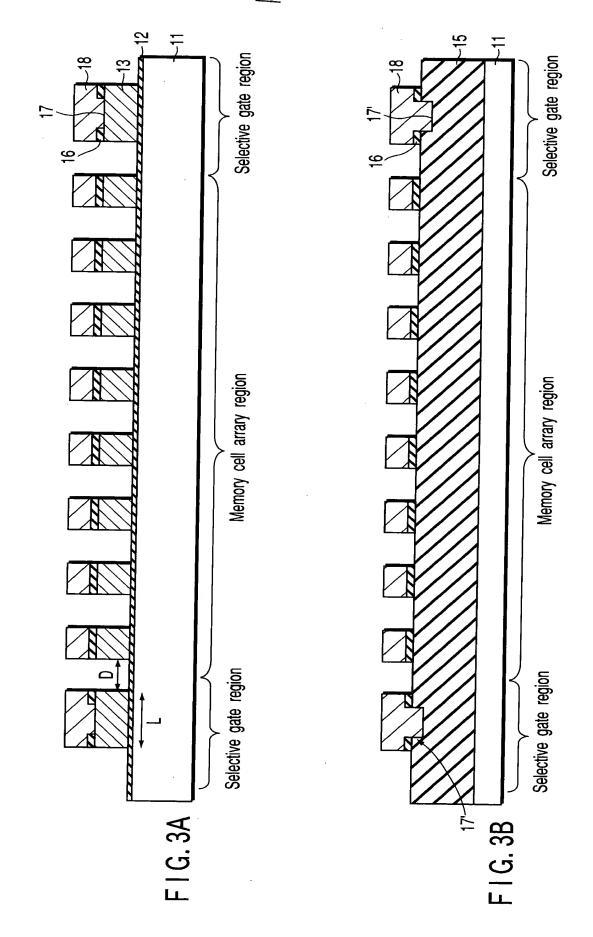


F I G. 2



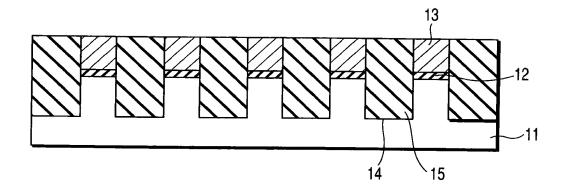
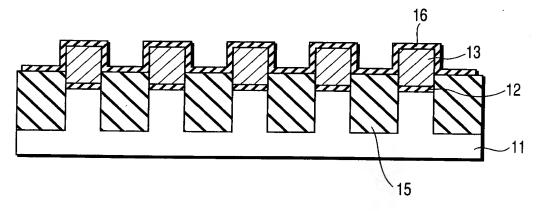
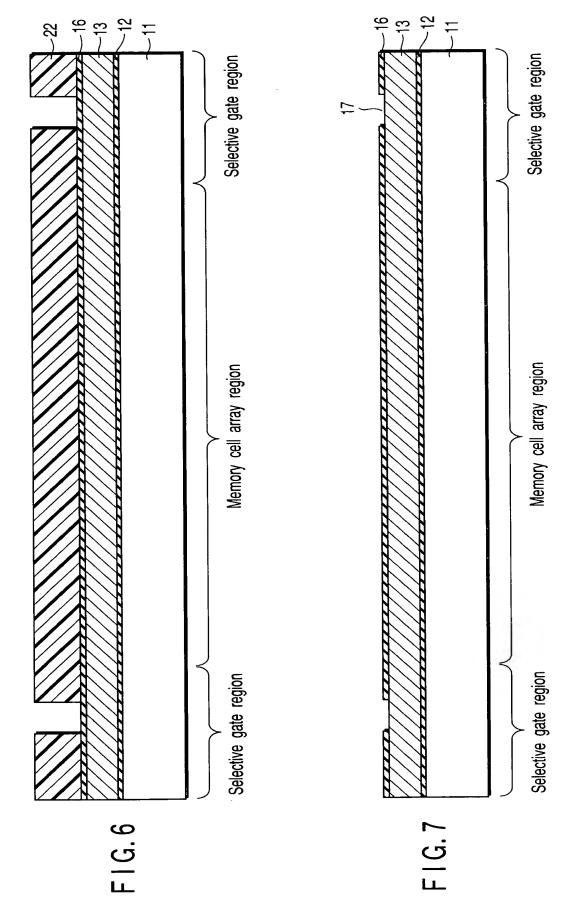
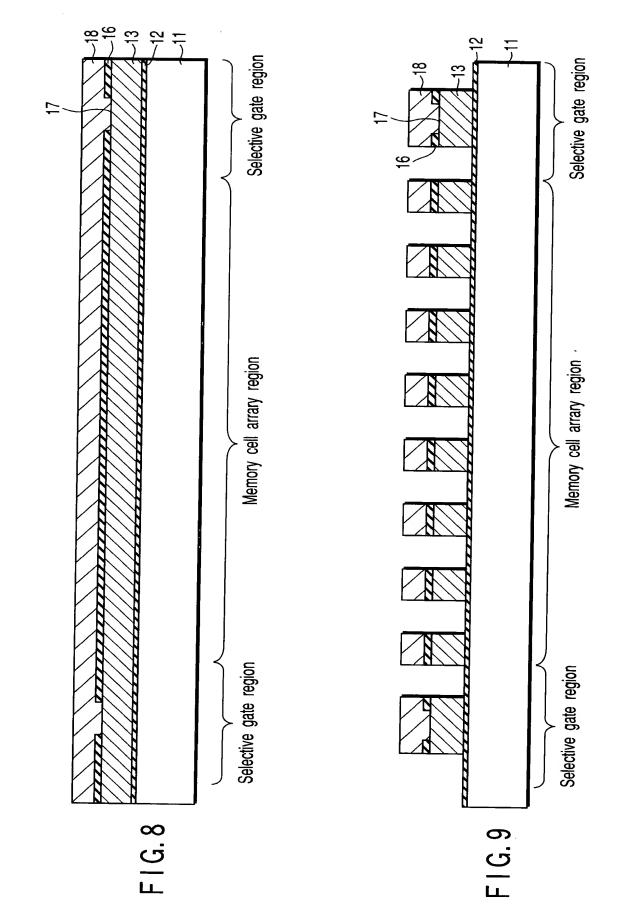


FIG.4



F I G. 5





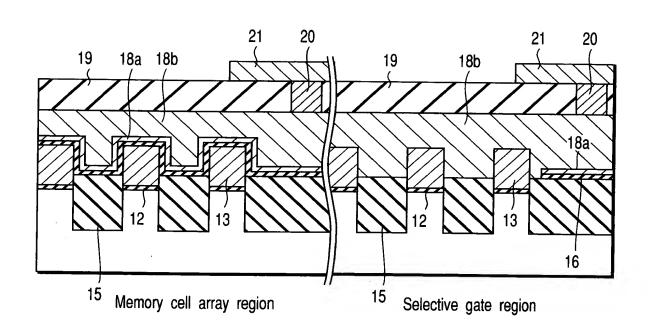
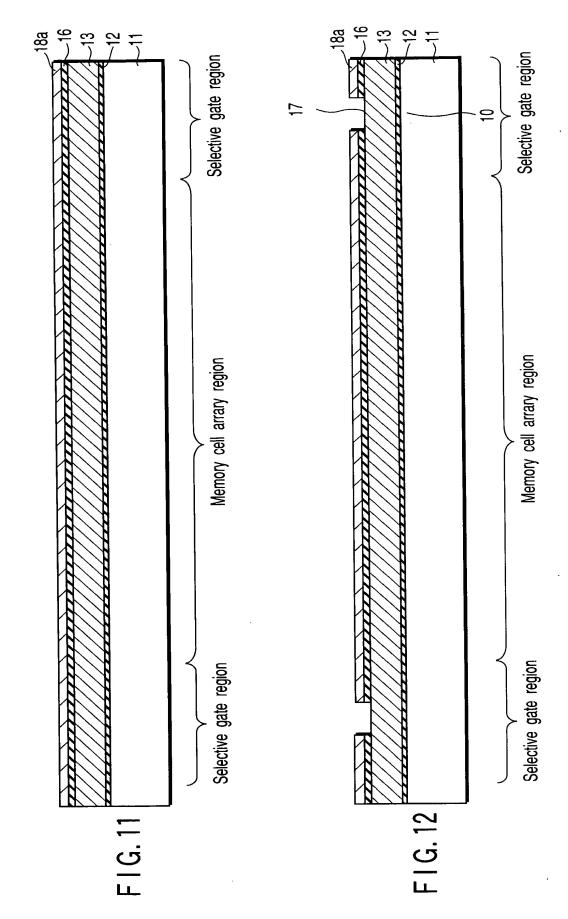
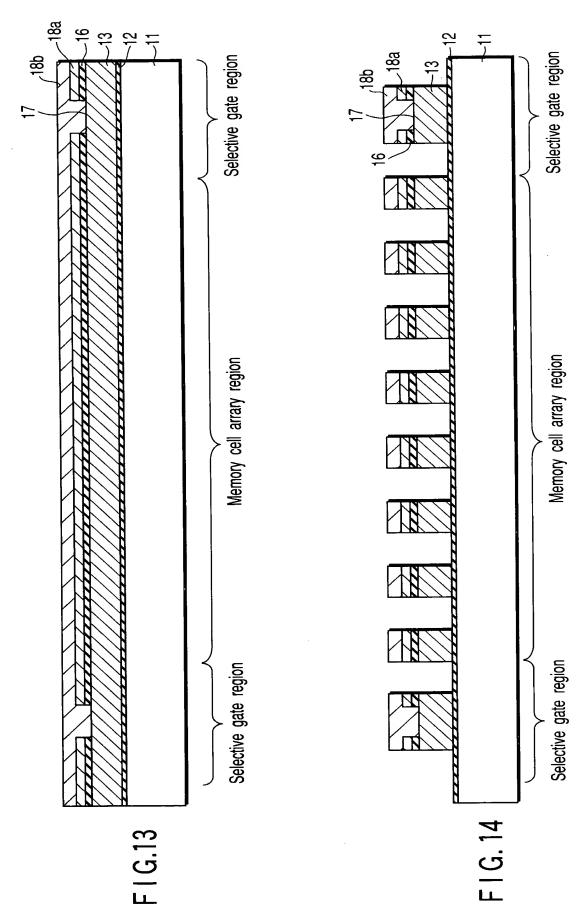
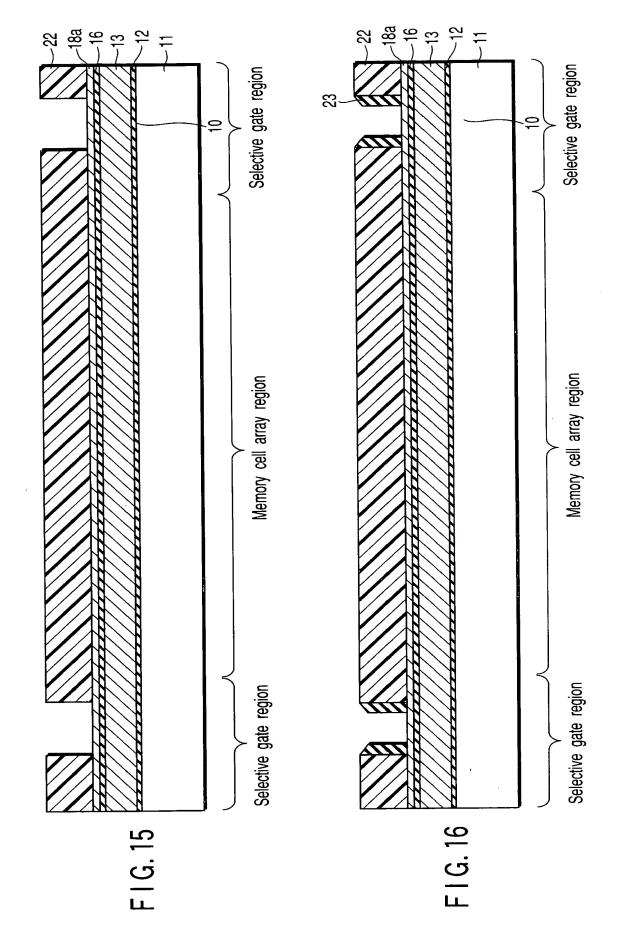
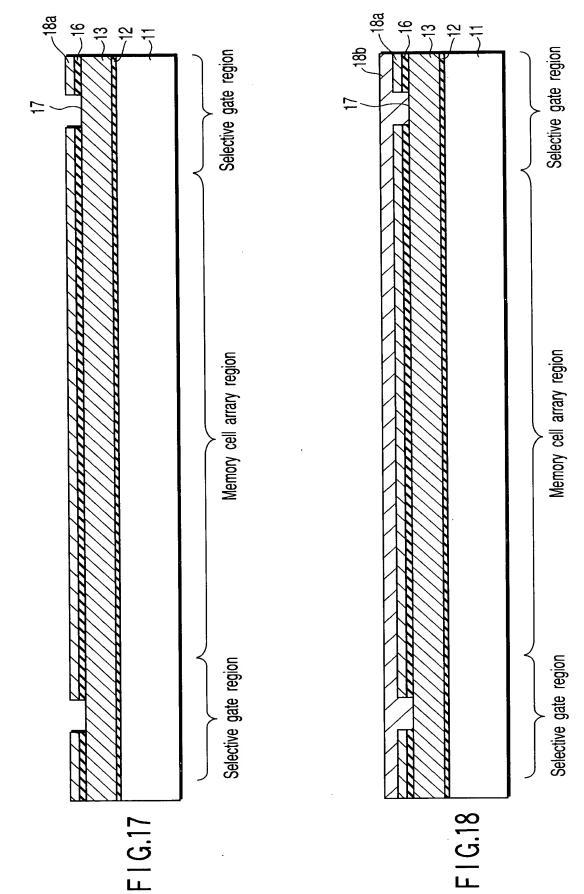


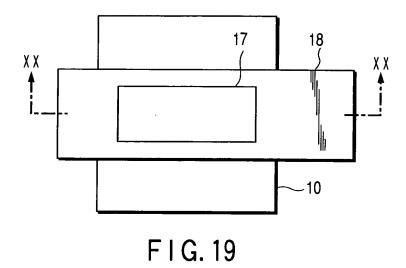
FIG. 10

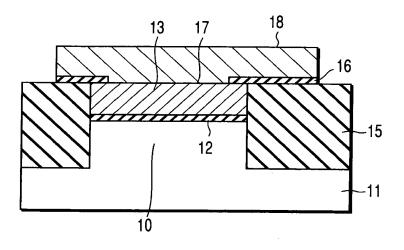




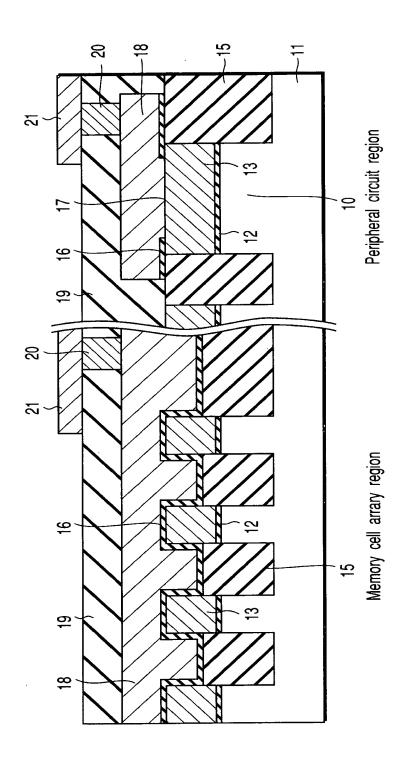




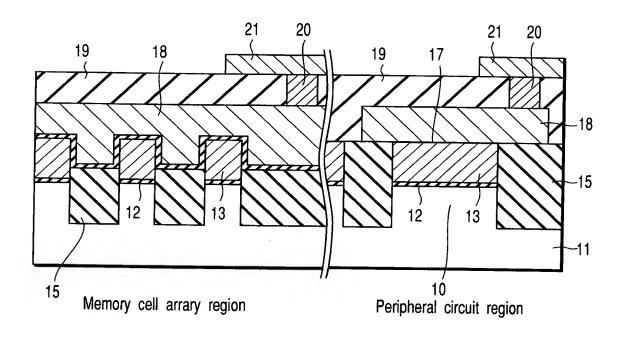




F I G. 20



F 1 G. 2



F I G. 22

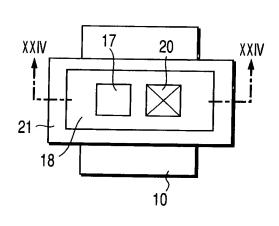


FIG. 23

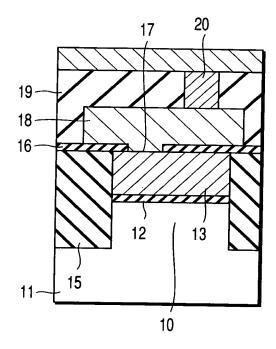
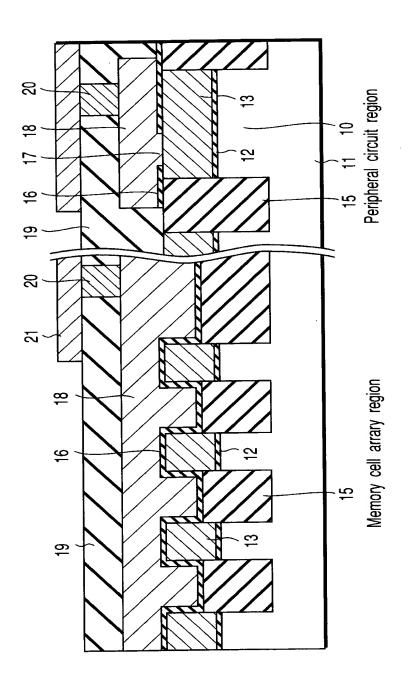
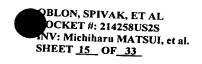


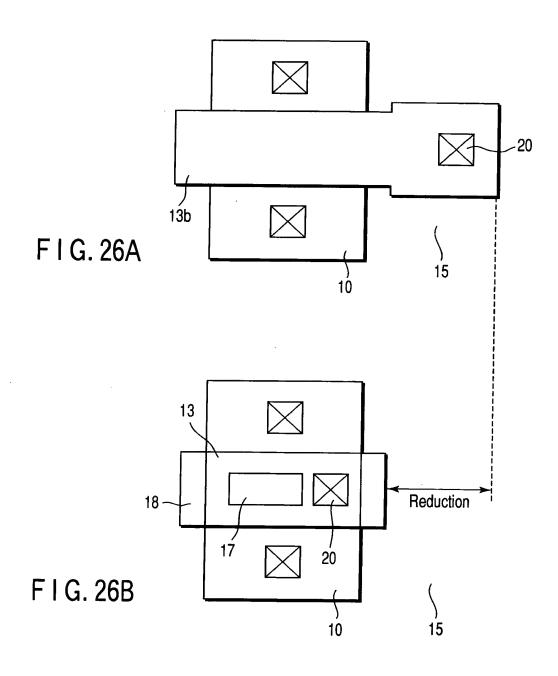
FIG. 24

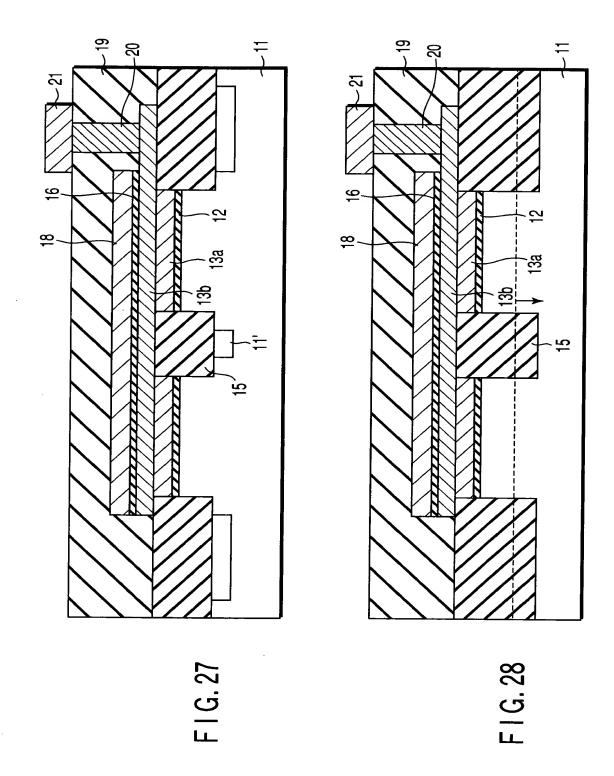
1

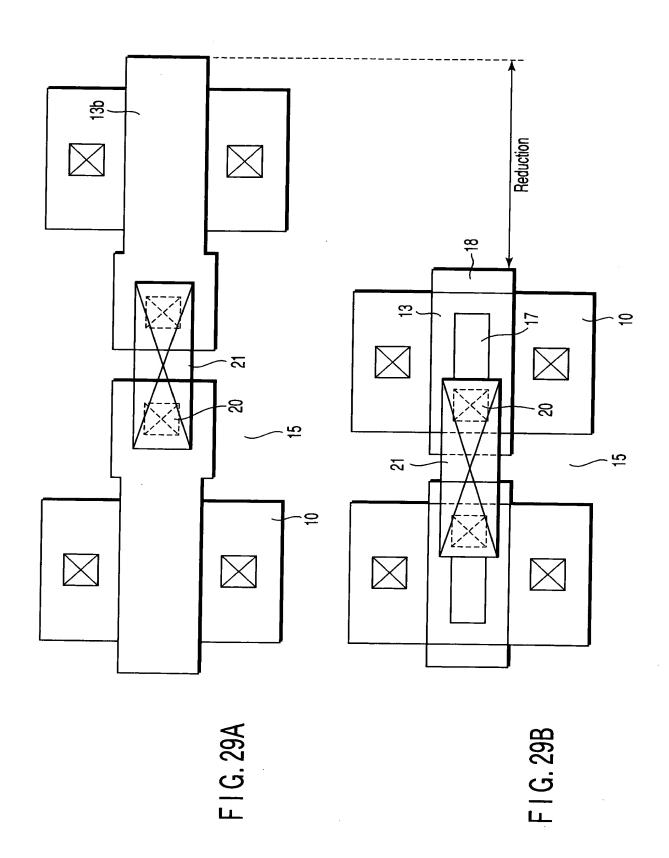


F1G.25

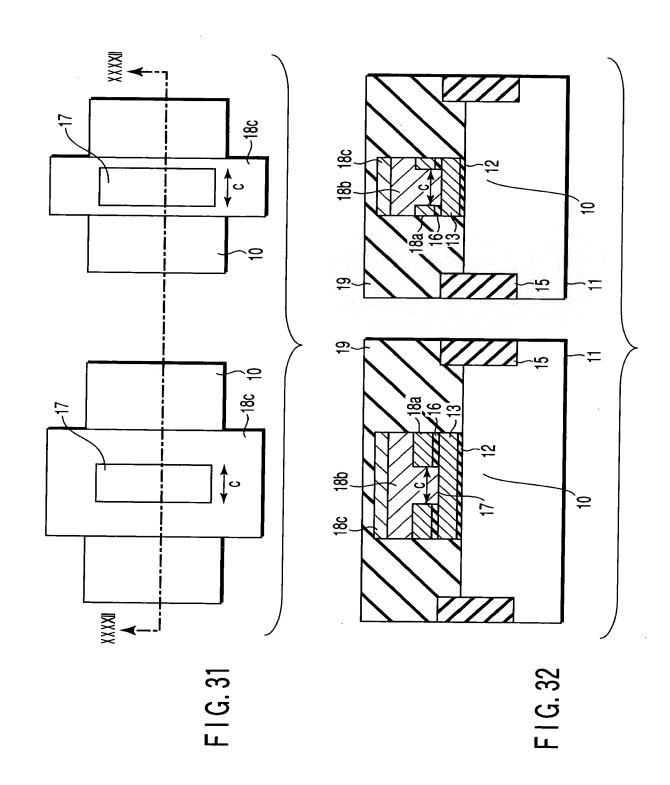


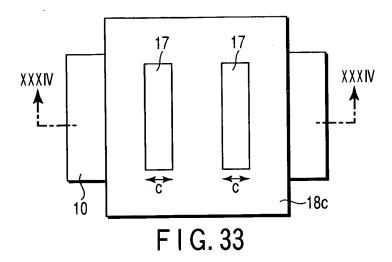


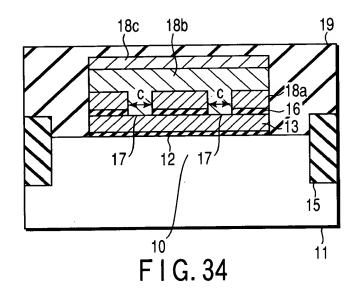


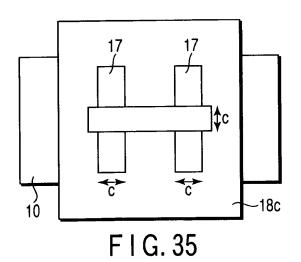


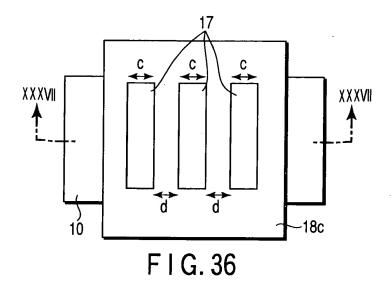
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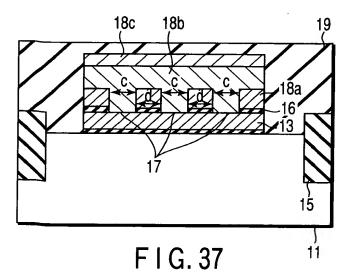


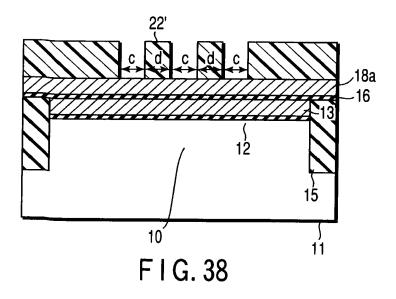


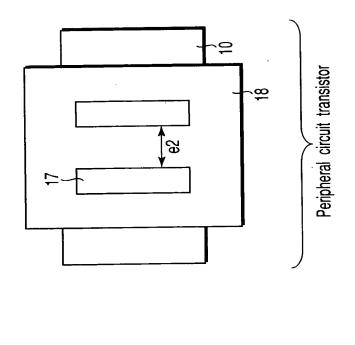








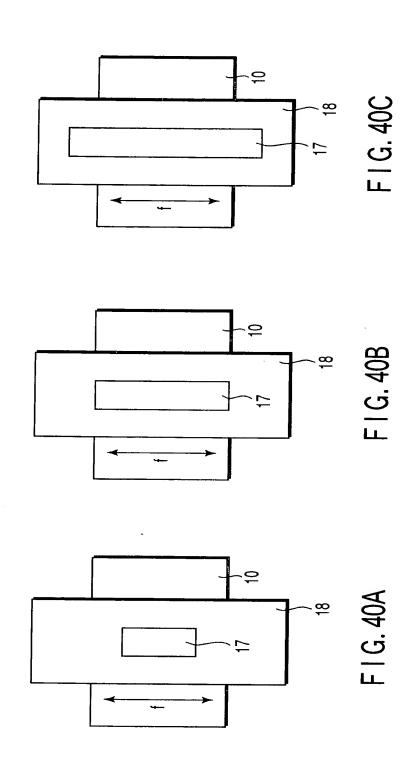




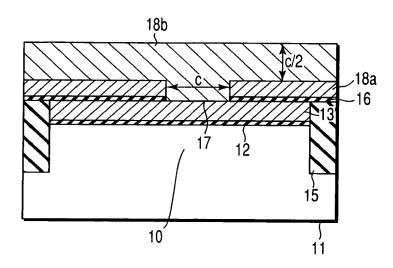
Selective transistor Memory transistor

FIG. 33

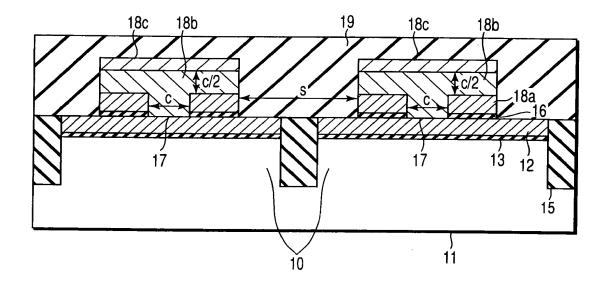
FIG. 39B



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F I G. 41A



F I G. 41B

F I G. 42A

17

12

13

15

10

11

F I G. 42B

17

18b

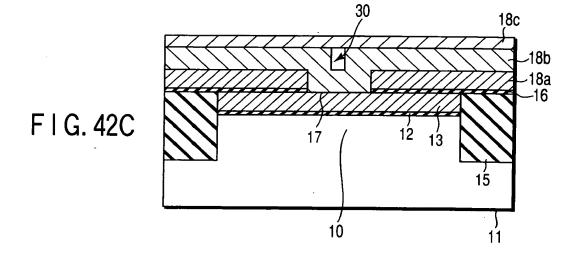
18a

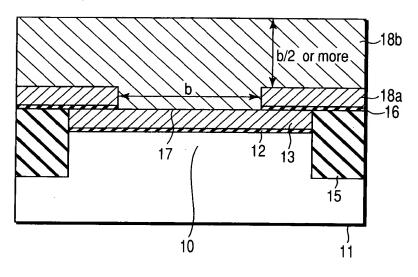
16

17

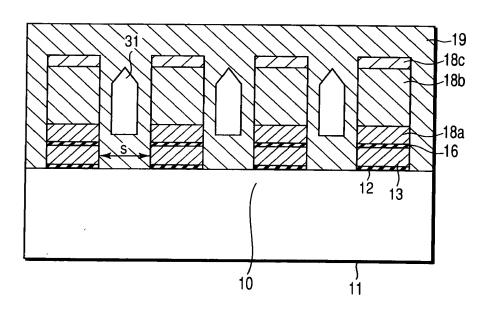
10

11



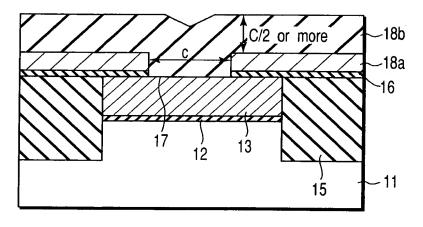


F I G. 43A



F I G. 43B

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F I G. 44A

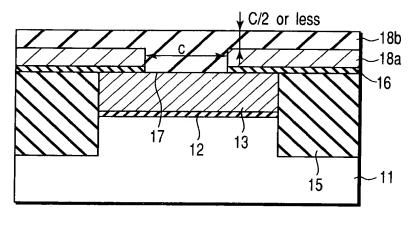


FIG. 44B

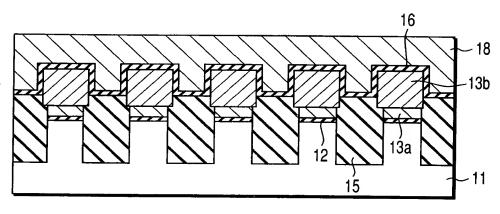
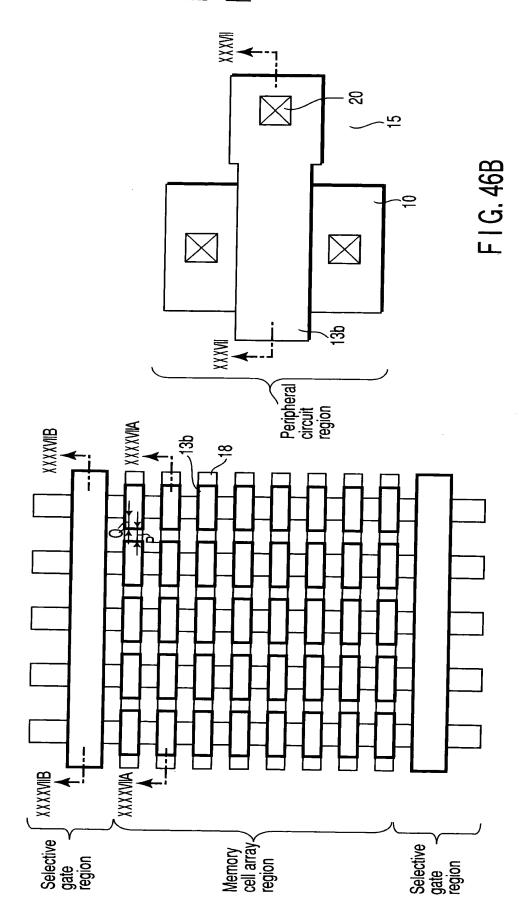
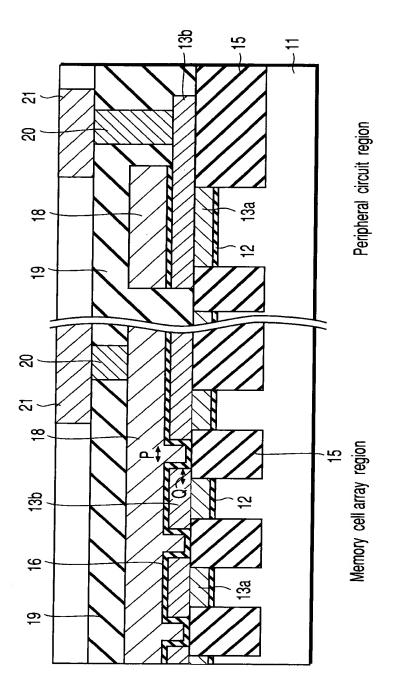


FIG. 45



F1G. 46A



F1G. 47A

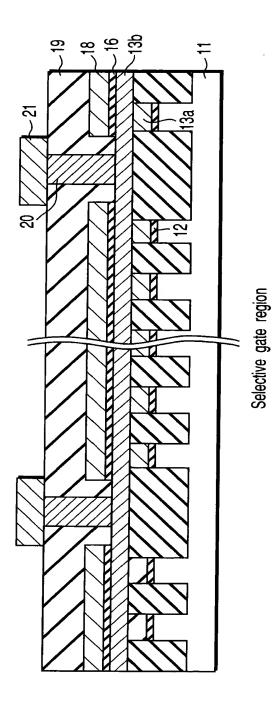
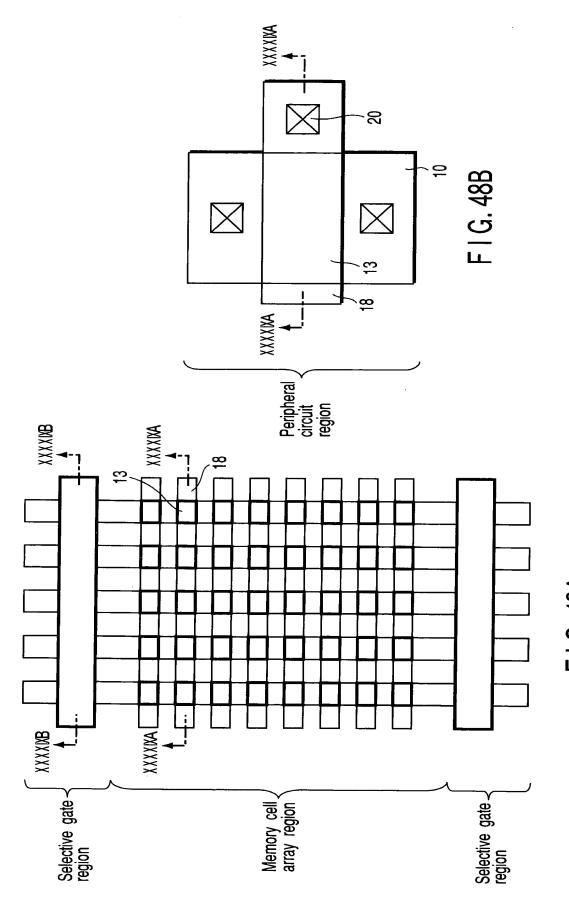


FIG. 47E

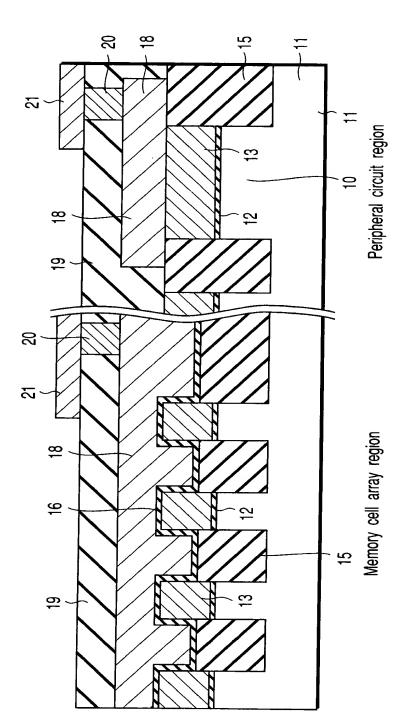






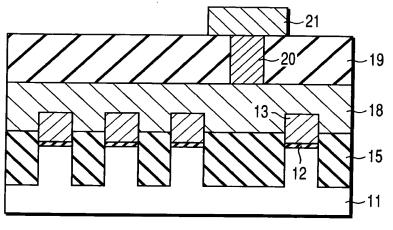
F1G. 48A

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F I G. 49A

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Selective gate region

FIG. 49B